Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-4 (Canceled)

Claim 5 (Currently Amended): A differential input section comprising:

a differential circuit having a first transistor and a second transistor, wherein source electrodes of the first and second transistors are connected to each other;

a first current mirror circuit connected to the first transistor;

a second current mirror circuit connected to the second transistor; and

a circuit that is connected to the first and second current mirror circuits and that is responsive to a voltage level of a signal output by the second current mirror circuit, so that a voltage level ~~levels~~ of a signal ~~signals~~ output by the first ~~and second~~ current mirror circuit becomes ~~circuits become~~ equal to ~~each other~~ the voltage level of the signal output by the second current mirror circuit.

Claim 6 (Previously Presented): The differential input section according to claim 5, wherein said circuit comprises:

a third transistor having a gate electrode connected to the second current mirror

circuit, a source electrode connected to a constant current source and a drain electrode coupled to a first voltage line; and

a fourth transistor having a gate electrode connected to the source electrode of the third transistor, a source electrode connected to the first current mirror circuit and a drain electrode coupled to a second voltage line.

Claim 7 (Previously Presented): The differential input section according to claim 6, wherein conductive types of said third and fourth transistors differ from each other.

Claim 8 (Previously Presented): The differential input section according to claim 7, wherein said third transistor is an N-type MOS transistor and wherein said fourth transistor is a P-type MOS transistor.

Claim 9 (Previously Presented): The differential input section according to claim 8, wherein said first transistor of the differential circuit further has a gate electrode having a first input signal coupled thereto and a drain electrode connected to the first current mirror circuit, and wherein said second transistor of the differential circuit further has a gate electrode having a second input signal coupled thereto and a drain electrode connected to the second current mirror circuit.

Claim 10 (Previously Presented): The differential input section according to claim 9,

wherein conductive types of said first and second transistors are the same.

Claim 11 (Previously Presented): The differential input section according to claim 10, wherein said first and second transistors are N-type MOS transistors.

Claim 12 (Previously Presented): The differential input section according to claim 8, wherein said first current mirror circuit comprises a fifth transistor and a sixth transistor each of which having respective gate electrodes connected to each other,

wherein said fifth transistor has a drain electrode connected to the first transistor of the differential circuit and a source electrode coupled to the first voltage line, and

wherein said sixth transistor has a drain electrode connected to the source electrode of the fourth transistor of the circuit and a source electrode coupled to the first voltage line.

Claim 13 (Previously Presented): The differential input section according to claim 12, wherein conductive types of said fifth and sixth transistors are the same.

Claim 14 (Previously Presented): The differential input section according to claim 13, wherein said fifth and sixth transistors are P-type MOS transistors.

Claim 15 (Previously Presented): The differential input section according to claim 8,

wherein said second current mirror circuit comprises a fifth transistor and a sixth transistor each of which having respective gate electrodes connected to each other,

wherein said fifth transistor has a drain electrode connected to the second transistor of the differential circuit and a source electrode coupled to the first voltage line, and

wherein said sixth transistor has a drain electrode connected to the gate electrode of the third transistor of the circuit and a source electrode coupled to the first voltage line.

Claim 16 (Previously Presented): The differential input section according to claim 15, wherein conductive types of said fifth and sixth transistors are the same.

Claim 17 (Previously Presented): The differential input section according to claim 16, wherein said fifth and sixth transistors are P-type MOS transistors.

Claim 18 (Previously Presented): The differential input section according to claim 7, wherein said third transistor is an N-type MOS transistor and wherein said fourth transistor is a P-type MOS transistor.

Claim 19 (Previously Presented): The differential input section according to claim 18, wherein said first transistor of the differential circuit further has a gate electrode having

a first input signal coupled thereto and a drain electrode connected to the first current mirror circuit, and wherein said second transistor of the differential circuit further has a gate electrode having a second input signal coupled thereto and a drain electrode connected to the second current mirror circuit.

Claim 20 (Previously Presented): The differential input section according to claim 19, wherein conductive types of said first and second transistors are the same.

Claim 21 (Previously Presented): The differential input section according to claim 20, wherein said first and second transistors are N-type MOS transistors.

Claim 22 (Previously Presented): The differential input section according to claim 18, wherein said first current mirror circuit comprises a fifth transistor and a sixth transistor each having respective gate electrodes connected to each other,

wherein said fifth transistor has a drain electrode connected to the first transistor of the differential circuit and a source electrode coupled to the first voltage line, and

wherein said sixth transistor has a drain electrode connected to the source electrode of the fourth transistor of the circuit and a source electrode coupled to the first voltage line.

Claim 23 (Previously Presented): The differential input section according to claim 22,

wherein conductive types of said fifth and sixth transistors are the same.

Claim 24 (Previously Presented): The differential input section according to claim 23, wherein said fifth and sixth transistors are P-type MOS transistors.

Claim 25 (Previously Presented): The differential input section according to claim 18, wherein said second current mirror circuit comprises a fifth transistor and a sixth transistor each having respective gate electrodes connected to each other,

wherein said fifth transistor has a drain electrode connected to the second transistor of the differential circuit and a source electrode coupled to the first voltage line, and

wherein said sixth transistor has a drain electrode connected to the gate electrode of the third transistor of the circuit and a source electrode coupled to the first voltage line.

Claim 26 (Previously Presented): The differential input section according to claim 25, wherein conductive types of said fifth and sixth transistors are the same.

Claim 27 (Previously Presented): The differential input section according to claim 26, wherein said fifth and sixth transistors are P-type MOS transistors.

Claim 28 (Previously Presented): A differential input section comprising:

a differential circuit having a first transistor and a second transistor, wherein source electrodes of the first and second transistors are connected to each other;

a first current mirror circuit having an input node and an output node, wherein the input node is connected to a drain electrode of the first transistor of the differential circuit;

a second current mirror circuit having an input node and an output node, wherein the input node of the second current mirror circuit is connected to a drain electrode of the second transistor of the differential circuit; and

a feedback circuit connected to the output nodes of the first and second current mirror circuits, wherein a voltage of the output node of the second current mirror circuit is supplied to the output node of the first current mirror circuit.

Claim 29 (Previously Presented): The differential input section according to claim 28, wherein said feedback circuit comprises:

a third transistor having a gate electrode connected to the output node of the second current mirror circuit, a source electrode connected to a constant current source and a drain electrode coupled to a first voltage line, wherein a voltage of the source electrode of the third transistor is supplied as a substrate bias of the third transistor; and

a fourth transistor having a gate electrode connected to the source electrode of the third transistor, a source electrode connected to the output node of the first current

mirror circuit and a drain electrode coupled to a second voltage line, wherein a voltage of the output node of the first current mirror circuit is supplied as a substrate bias of the fourth transistor.

Claim 30 (Previously Presented): An operational amplifier comprising:

a differential input section comprising

a differential circuit having a first transistor and a second transistor, wherein source electrodes of the first and second transistors are connected to each other,

a first current mirror circuit having an input node and an output node, wherein the input node is connected to a drain electrode of the first transistor of the differential circuit,

a second current mirror circuit having an input node and an output node, wherein the input node of the second current mirror circuit is connected to a drain electrode of the second transistor of the differential circuit, and

a feedback circuit connected to the output nodes of the first and second current mirror circuits, wherein a voltage of the output node of the second current mirror circuit is supplied to the output node of the first current mirror circuit;

an amplifying section having an input node connected to the output node of the second current mirror circuit and having an output node, wherein the amplifying section amplifies a voltage level of the output node of the second current mirror circuit; and

an output section having an input node connected to the output node of the amplifying section and an output node connected to an output terminal, wherein the output section generates a voltage according to the voltage level of the output node of the second current mirror circuit and a voltage level of the output node of the amplifying section.

Claim 31 (Previously Presented): The operational amplifier according to claim 30, wherein the voltage level of the output node of the second current mirror circuit increases when the voltage level of the output node of the amplifying section decreases.

Claim 32 (Previously Presented): The operational amplifier according to claim 30, wherein the voltage level of the output node of the second current mirror decreases when the voltage level of the output node of the amplifying section increases.